Claims

1. A level shifter for use in thin film transistor liquid crystal displays (TFT-LCD), comprising:

   a shift circuit for shifting from an input voltage level to an output voltage level, comprising:

      a first transistor comprising a source, a drain, a gate, and a body; and

      a second transistor comprising a source, a drain, a gate, and a body; and

   a first bias circuit, comprising an input terminal and an output terminal;

   wherein the output terminal of the first bias circuit is connected to the body of the first transistor to adjust a threshold voltage of the first transistor according to the input voltage level.

2. The level shifter of claim 1, wherein the first transistor and the second transistor are both n-channel TFTs.

3. The level shifter of claim 2, further comprising a second bias circuit, comprising an input terminal and an output terminal, for biasing the body of the second transistor, the shift circuit comprises:

   a first input terminal for inputting the input voltage level;

   a second input terminal for inputting the input voltage level but with opposite phase;

   a third transistor being a p-channel TFT and comprising a source, a drain, and a gate; and

   a fourth transistor being a p-channel TFT and comprising a source, a drain, and a gate;

   wherein the input terminal of the first bias circuit is connected to the gate of the first transistor, the input terminal of the second bias circuit is connected to the gate of the second transistor, the sources of the first transistor and the second transistor are both grounded, the gate of the first transistor is connected to the

first input terminal, the drain of the first transistor is connected to the drain of the third transistor, the gate of the second transistor is connected to the second input terminal, the drain of second transistor is connected to the drain of the fourth transistor, the gate of the third transistor is connected to the drain of the third transistor, the gate of the fourth transistor is connected to the gate of the third transistor, the sources of the third transistor and the fourth transistor are both connected to a power supply, and the output voltage level is extracted from the drain of the fourth transistor.

4. The level shifter of claim 2, further comprising a second bias circuit, comprising an input terminal and an output terminal, for biasing the body of the second transistor, the shift circuit comprises:

a first input terminal for inputting the input voltage level;

a second input terminal for inputting the input voltage level but with opposite phase;

a third transistor being a p-channel TFT and comprising a source, a drain, and a gate; and

a fourth transistor being a p-channel TFT and comprising a source, a drain, and a gate;

wherein the input terminal of the first bias circuit is connected to the gate of the first transistor, the input terminal of the second bias circuit is connected to the gate of the second transistor, the sources of the first transistor and the second transistor are both grounded, the gate of the first transistor is connected to the first input terminal, the drain of the first transistor is connected to the drain of the third transistor, the gate of the second transistor is connected to the second input terminal, the drain of the second transistor is connected to the drain of the fourth transistor, the gate of the third transistor is connected to the drain of the fourth transistor, the gate of the fourth transistor is connected to the drain of the

third transistor, the sources of the third transistor and the fourth transistor are both connected to a power supply, and the output voltage level is extracted from the drain of the fourth transistor.

5. The level shifter of claim 2, further comprising a second bias circuit, comprising an input terminal and an output terminal, for biasing the body of the second transistor, the shift circuit comprises:

an input terminal for inputting the input voltage level;

a third transistor being a p-channel TFT and comprising a source, a drain, and a gate; and

a fourth transistor being a p-channel TFT and comprising a source, a drain, and a gate;

wherein the input terminals of the first bias circuit and the second bias circuit are both connected to the gate of the first transistor, the sources of the first transistor and the second transistor are both grounded, the gate of the first transistor is connected to the input terminal of the shift circuit, the drain of the first transistor is connected to the drain of the third transistor, the gate of the second transistor is connected to the body of the second transistor, the drain of the second transistor is connected to the drain of the fourth transistor, the gate of the third transistor is connected to the drain of the third transistor, the gate of the fourth transistor is connected to the gate of the third transistor, the sources of the third transistor and the fourth transistor are both connected to a power supply, and the output voltage level is extracted from the drain of the fourth transistor.

6. The level shifter of claim 3, 4, or 5, wherein the first bias circuit comprises an inverter.

7. The level shifter of claim 3, 4, or 5, wherein the second bias circuit comprises an

inverter.

8. A level shifter for use in TFT-LCDs, comprising:

a shift circuit for shifting from an input voltage level to an output voltage level, comprising:

a first transistor being a n-channel TFT and comprising a source, a drain, a gate, and a body;

a second transistor being a n-channel TFT and comprising a source, a drain, a gate, and a body;

a third transistor being a p-channel TFT and comprising a source, a drain, and a gate; and

a fourth transistor being a p-channel TFT and comprising a source, a drain, and a gate; and

a first bias circuit, comprising an input terminal and an output terminal;

wherein the output terminal of the first bias circuit is connected to the body of the first transistor to adjust a threshold voltage of the first transistor according to the input voltage level.

9. The level shifter of claim 8, further comprising a second bias circuit, comprising an input terminal and an output terminal, for biasing the body of the second transistor, the shift circuit comprises:

a first input terminal for inputting the input voltage level; and

a second input terminal for inputting the input voltage level but with opposite phase;

wherein the input terminal of the first bias circuit is connected to the gate of the first transistor, the input terminal of the second bias circuit is connected to the gate of the second transistor, the sources of the first transistor and the second transistor are both grounded, the gate of the first transistor is connected to the

first input terminal, the drain of the first transistor is connected to the drain of the third transistor, the gate of the second transistor is connected to the second input terminal, the drain of second transistor is connected to the drain of the fourth transistor, the gate of the third transistor is connected to the drain of the third transistor, the gate of the fourth transistor is connected to the gate of the third transistor, the sources of the third transistor and the fourth transistor are both connected to a power supply, and the output voltage level is extracted from the drain of the fourth transistor.

10. The level shifter of claim 8, further comprising a second bias circuit, comprising an input terminal and an output terminal, for biasing the body of the second transistor, the shift circuit comprises:

a first input terminal for inputting the input voltage level; and

a second input terminal for inputting the input voltage level but with opposite phase;

wherein the input terminal of the first bias circuit is connected to the gate of the first transistor, the input terminal of the second bias circuit is connected to the gate of the second transistor, the sources of the first transistor and the second transistor are both grounded, the gate of the first transistor is connected to the first input terminal, the drain of the first transistor is connected to the drain of the third transistor, the gate of the second transistor is connected to the second input terminal, the drain of the second transistor is connected to the drain of the fourth transistor, the gate of the third transistor is connected to the drain of the fourth transistor, the gate of the fourth transistor is connected to the drain of the third transistor, the sources of the third transistor and the fourth transistor are both connected to a power supply, and the output voltage level is extracted from the drain of the fourth transistor.

11. The level shifter of claim 8, further comprising a second bias circuit, comprising an input terminal and an output terminal, for biasing the body of the second transistor, the shift circuit comprises:

an input terminal for inputting the input voltage level;

wherein the input terminals of the first bias circuit and the second bias circuit are both connected to the gate of the first transistor, the sources of the first transistor and the second transistor are both grounded, the gate of the first transistor is connected to the input terminal of the shift circuit, the drain of the first transistor is connected to the drain of the third transistor, the gate of the second transistor is connected to the body of the second transistor, the drain of the second transistor is connected to the drain of the fourth transistor, the gate of the third transistor is connected to the drain of the third transistor, the gate of the fourth transistor is connected to the gate of the third transistor, the sources of the third transistor and the fourth transistor are both connected to a power supply, and the output voltage level is extracted from the drain of the fourth transistor.

12. The level shifter of claim 9, 10, or 11, wherein the first bias circuit comprises an inverter.

13. The level shifter of claim 9, 10, or 11, wherein the second bias circuit comprises an inverter.

14. A level shifter for use in TFT-LCDs, comprising:

a first input terminal for inputting the input voltage level;

a second input terminal for inputting the input voltage level but with opposite phase;

a shift circuit for shifting from an input voltage level to an output voltage level, comprising:

a first transistor being a n-channel TFT and comprising a source, a drain, a gate, and a body;

a second transistor being a n-channel TFT and comprising a source, a drain, a gate, and a body;

a third transistor being a p-channel TFT and comprising a source, a drain, and a gate; and

a fourth transistor being a p-channel TFT and comprising a source, a drain, and a gate;

a first bias circuit, comprising an input terminal and an output terminal, for biasing the body of the first transistor; and

a second bias circuit, comprising an input terminal and an output terminal, for biasing the body of the second transistor;

wherein the input terminal of the first bias circuit is connected to the gate of the first transistor, the input terminal of the second bias circuit is connected to the gate of the second transistor, the output terminal of the first bias circuit is connected to the body of the first transistor, the output terminal of the second bias circuit is connected to the body of the second transistor, the gate of the first transistor is connected to the first input terminal, and the gate of the second transistor is connected to the second input terminal.

15. The level shifter of claim 14, wherein the sources of the first transistor and the second transistor are both grounded, the drain of the first transistor is connected to the drain of the third transistor, the drain of second transistor is connected to the drain of the fourth transistor, the gate of the third transistor is connected to the drain of the third transistor, the gate of the fourth transistor is connected to the gate of the third transistor, the sources of the third transistor and the fourth transistor are both

connected to a power supply, and the output voltage level is extracted from the drain of the fourth transistor.

16. The level shifter of claim 14, wherein the sources of the first transistor and the second transistor are both grounded, the drain of the first transistor is connected to the drain of the third transistor, the drain of the second transistor is connected to the drain of the fourth transistor, the gate of the third transistor is connected to the drain of the fourth transistor, the gate of the fourth transistor is connected to the drain of the third transistor, the sources of the third transistor and the fourth transistor are both connected to a power supply, and the output voltage level is extracted from the drain of the fourth transistor.
17. The level shifter of claim 15 or 16, wherein the first bias circuit comprises an inverter.
18. The level shifter of claim 15 or 16, wherein the second bias circuit comprises an inverter.